

# 1 Gb/s Fiber Optic Transmitter Design using Intersil Digitally Controlled Potentiometer (XDCP®) ICs

**Application Note** 

June 28, 2005

AN140.0

Authors: Joe Ciancio, Product Development Engineer, Rex Niven, Design Engineer, Forty Trout Electronics Pty. Ltd.

#### **Abstract**

Laser Diode (LD) controller/driver IC's at gigabit data-rates typically use specially designed chipsets. In many cases numerous control parameters are required to be set, using resistors which define reference or control currents used by the LD driver circuit. Precise and dependable settings are essential in order to achieve a maximized extinction ratio and minimize jitter.

Intersil Digitally Controlled Potentiometers (XDCPs) allow automated setting of these resistor values in a manner which is rapid, stable, repeatable and precise.

In addition, Intersil XDCPs offer many other integrated features such as EEPROM and trip alarms.

#### Introduction

Optical fiber communication systems often use semiconductor light sources such as a laser diode (LD) or light emitting diode (LED). Both have the advantage that the digital modulation at logic circuit voltages can be directly applied to the operating bias current of the diode, which in turn varies the output power. Laser diodes have advantages for communication systems, since they provide high coupled output power and routinely have high cutoff frequencies which allow for data rates in excess of 10Gb/s. Such high rates, call for purpose-designed circuits to control laser diode currents. A challenge for control circuits is the knee or threshold effect, below which optical output is minimal as shown in Figure 1.

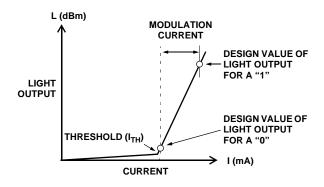


FIGURE 1. IDEALIZED LIGHT OUTPUT vs. CONTROL CURRENT

Many such chipsets for laser diode control exist, most sharing a similar architecture. This comprises a transistor which sets a bias current, another transistor providing extra current to modulate the laser diode into the '1' (maximum power) condition, and a common-emitter differential transistor pair switch. The function of this switch is to divert the modulation current away from the laser diode when a '0' is required. The differential pair can be directly controlled from an ECL or PECL input (Figure 2).

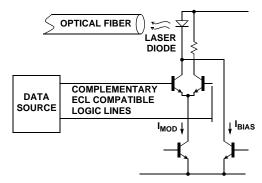


FIGURE 2. LASER DIODE DRIVER BLOCK DIAGRAM

The '1' level is often set near the maximum safe level of laser diode power output, while the '0' is set close to the threshold current (I<sub>TH</sub>), since this allows higher data rates. In practice a small amount light is expected at the '0' level since the "knee" at the threshold of the Light versus Current (L vs. I) characteristic curve is somewhat rounded.

Laser diodes exhibit a very wide range of tolerances of their various parameters, and this requires a number of reference values to be adapted to suit the individual component. In addition these values vary significantly with temperature.

The bias current  $(I_B)$  is controlled by a feedback loop from the laser diode's monitor diode (Refer to Figure 3).

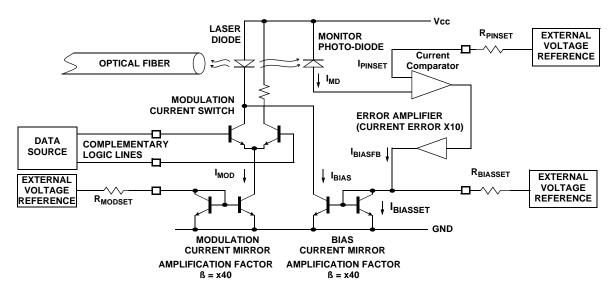


FIGURE 3. SY88922 LASER DIODE DRIVER AND SY88905 LASER DIODE CONTROLLER BLOCK DIAGRAM

The monitor photo-diode and feedback loop cannot "track" the optical signal at full data rate. Therefore, the bias feedback loop is designed such that it maintains an *average* optical power, which is influenced by the relative number of data '1's and '0's. The number of data '1's and '0's may be made consistent by employing a line code such as simple Manchester Coding, or more efficient, OMIT "8B/10B" Coding - as used in GBIC (fiber channel) transceiver modules.

As previously mentioned, at high data rates the modulation current ( $I_{MOD}$ ) cannot have feedback control, and must be set at a constant level. This therefore imposes the requirement that the modulation current must be desensitized OMIT, to the effects of temperature fluctuations and device ageing. In the schematic shown in Figure 3, the modulation current is set by choosing the appropriate value of  $R_{MODSFT}$ .

An example of the effect of temperature variation, is to reduce the gradient of the Light versus Current (L vs. I) characteristic curve of the laser diode. This is referred to as reduced *slope efficiency*. The lower slope efficiency has the

potential effect of making the laser diode in '0' condition transmit significant light power, while also reducing the power of the optical '1' level (Figure 4).

This approaching of the two levels reduces the *extinction* ratio (the '0' optical power level as a fraction of the '1' optical power level), which has a detrimental effect on the theoretical bit error rate (BER) by reducing the size of the "eye diagram" opening (Figure 5) [1].

To achieve a BER smaller than 1 x  $10^{-10}$ , requires the '1' signal level to be at least  $12.5\sigma$  (standard deviations) greater than the received noise. Should the '0' level rise to approach one standard noise deviation, the BER will deteriorate markedly. Therefore, the extinction ratio must be maximized for optimum results, although this must be balanced against the need for the zero level to be as far above threshold as possible to avoid bit-pattern dependent jitter [2]. This is achieved by reliable, and precise setting of the various control circuit parameters. These control parameters are usually currents, which are set/programmed by adjustable resistors.

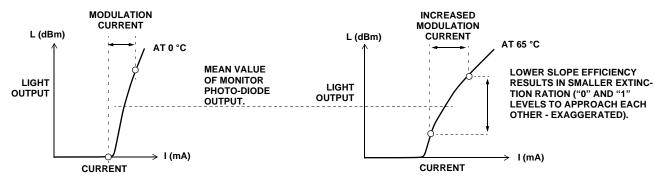


FIGURE 4. EFFECT OF REDUCED SLOPE EFFICIENCY DUE TO LASER DIODE TEMPERATURE VARIATION

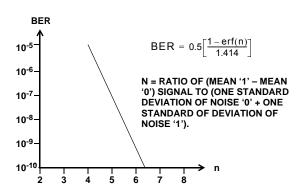


FIGURE 5. BIT ERROR RATE AS A FUNCTION OF SIGNAL TO NOISE RATIO

## Intersil Digitally Controlled Potentiometers in Laser Diode Driver Control

Ideally the resistors used to program/set the laser diode driver circuit parameters, should have the properties of:

- · Have high resolution
- · Allow adjustment over a wide range of resistance
- · Be ready immediately after power-up
- · Have low temperature coefficient
- · Be immune to vibration and shocks
- Introduce minimal noise, both internally generated and coupled from the exterior
- · Have low "wiper" resistance
- Be very stable with age and other environmental conditions
- · Be tamper proof
- Allow readjustment many times (at circuit set up time, for maintenance, or regular checkups)
- Permit a given setting to be reproduced with high accuracy
- Have a small footprint for use in small form-factor transceiver modules
- Avoid out-of-range values which may overdrive (and possibly damage) critical components such as the laser diode
- Readily allow automatic adjustment under digital/computer control
- · Allow multiple units in one package
- Be integrated with other ancillary functions
- Require no additional power supplies other than those available for other system functions
- Be non-volatile (does not require power to retain resistor settings)

 Allow a link to documentation of settings, with time/date stamp, serial number and operator data

The Intersil Digitally Controlled Potentiometer (XDCP) products offer all these features, and most will be shown in the example design below.

## Laser Diode Driver Circuit Design

In this circuit design example, the laser diode is controlled by the Micrel-Synergy chipset SY88922 and SY88905. This chipset uses PECL compatible data signals, and reference voltages (less control circuit input bias) of 1.0V. The laser diode used is a Vertical Cavity Surface Emitting Laser (VCSEL) with monitor diode, type Honeywell HFE4380-321. The complete schematic for this laser diode driver circuit is shown in the Appendix.

The VCSEL has some favorable characteristics compared to the more traditional plane cavity (edge-emitter) type laser diodes. For example, a VCSEL has the properties of

- · Lower threshold current
- Less influence of temperature on threshold current, with a minimum near room temperature [3]
- · Critically-damped relaxation oscillation
- Only one longitudinal mode, giving narrow spectral width
  [4]

Some important characteristics of the HFE4380-321 are summarized in Table 1 and Table 2.

TABLE 1. KEY PARAMETERS OF VCSEL HFE4380-321

	MIN	TYP	MAX	UNITS
Optical Power Output	0.2	0.35	0.8	mW
Threshold	-	3.5	6	mA
Slope efficiency	0.02	0.04	0.1	mW/mA
Monitor current (at 0.35mW optical)	0.07		0.275	mA
Series resistance	15	25	50	Ω
Forward voltage	1.6	1.8	2.2	V

TABLE 2. TEMP. DEPENDENCY OF VCSEL HFE4380-321

	MIN	TYP	MAX	UNITS
Threshold (1)				mA
	-1		+1	(0 to 70°C)
Slope efficiency		-0.4		%/°C
Monitor current		+0.2		%/°C

 The threshold varies parabolically with temperature having a minimum at mid range of temperature (around +30°C). Some precautions to be observed with VCSELs are:

- The zero point should be as far as possible above threshold to prevent very long tails of the falling edges and bit-pattern dependent jitter [5].
- The fiber coupling and fiber should not favour one polarization or transverse mode as this may result in pulse distortion such as large overshoot or undershoot at the rising edge and zero bounce after the falling edge [6].
- Optical reflections from the fiber to the laser should be minimized (as for edge emitters)

## Selecting Resistor Values

In setting the various control circuit parameters, allowance must be made for maximum and minimum values, as shown in Table 3. The calculated resistor values are shown in Table 4.

TABLE 3. PARAMETERS OF SY88922 & SY88905 CHIPSET

	MIN	TYP	MAX	UNITS
$\Delta V_{PINSET}$	0.95	1.13	1.35	V
$\Delta V_{BIASSET}$	0.8	1.0	1.2	V
ß <sub>BIAS</sub>	28	37	44	μΑ/μΑ
ß <sub>MOD</sub>	30	38	44	μΑ/μΑ

**TABLE 4. RANGE OF CALCULATED RESISTOR VALUES** 

	MIN	<b>-3</b> σ	TYP	<b>-3</b> σ	MAX	UNITS
R <sub>PINSET</sub> (R7)	6.9	7.2	14.4	29	38.6	kΩ
R <sub>BIASSET</sub> (R8)	4.5	6.9	10.6	16	21.1	kΩ
R <sub>MODSET</sub> (R6)	1.4	2.0	4.3	9.5	15.1	kΩ

An initial design decision is that the laser diode will be operated at the nominal value of 0.35mW. Also, operation is assumed to be at 25°C.

To calculate the range of resistor values required, some basic design equations are required:

$$I_{PIN} = \left(\frac{\Delta V_{PINSET}}{R_{PINSET}}\right) - 1$$

(we assume zero error current in nominal conditions with normal data signal being transmitted)

$$\Delta V_{PINSET} = V_{PINSET} - V_{INM}$$
 \_\_\_\_\_2

V<sub>INM</sub> = input voltage of current mirror

I<sub>PIN</sub> = monitor photo-diode current

With the laser diode giving the optical power output "P<sub>1</sub>" at a '1' level, and with an equal number of '1's and '0's, the monitor current will be 50% of the full-power value.

$$I_{\text{BIAS}} = \left(\frac{\beta_{\text{BIAS}} \Delta V_{\text{BIASSET}}}{R_{\text{BIASSET}}}\right) I_{\text{TH}}$$
 —3

$$\Delta V_{\text{BIASSET}} = V_{\text{BIASSET}} - V_{\text{INM}}$$

V<sub>INM</sub> = input voltage of current mirror

 $\beta_{BIAS}$  = bias current mirror gain

$$\frac{P_1}{(\eta \beta_{MOD})} = \left(\frac{\Delta V_{MODSET}}{R_{MODSET}}\right)$$

P<sub>1</sub> = nominal optical output power of a '1'

η = slope efficiency

 $\beta_{MOD}$  = modulation current mirror gain

Each resistor (R6, R7, R8) depends upon three or more parameters, some of which can have tolerances as high as (+100% / -50%). For example, a simple calculation of minimum and maximum values for  $R_{\mbox{\scriptsize MODSET}}$  reveals a potential range of values of 10:1.

However, common-sense engineering would dictate that absolute minimum or maximum possible values represent the combination of the "three-sigma"  $(3\sigma)$  limit of every component - an extremely unlikely scenario, or gross overdesign! An approach which acknowledges the statistical nature of product parameter distributions would use a root-mean-square method, where the square root of the sum of the squares of the possible variation (in relative terms) is calculated. Even the three sigma limit could be considered overkill, since a two-sigma threshold still gives 95% of products within the design range.

This approach assumes a normal or gaussian distribution for each parameter. For components which are selected from a population with a much wider distribution, this may not be valid. For parameters which vary over a 4:1 range, this method is obviously only approximate.

For the laser diode selected however, the distribution of threshold is indeed close to Gaussian form [7].

#### Temperature Effects

The potential temperature variation of the circuit must be known. Using the known laser diode and control circuit temperature sensitivity (see Table 2), the range of the error amplifier gain (used to correct for changes in necessary bias current) should be checked.

A rise in temperature causes the slope efficiency to drop (-0.4%/ $^{\circ}$ C), normally causing the '0' level to rise. However, the increase in monitor current (+0.2%/ $^{\circ}$ C) will partly compensate for this effect.

#### Other Resistors

A resistor (R5) in series with the complementary transistor in the current switch is used to approximately match the conduction conditions of the other transistor. It is also useful since it allows an oscilloscope to check the drive current waveform which should be similar to that of the laser diode.

## Applying Intersil Digitally Controlled Potentiometers

Given the wide range of variables, it is desired to set the three resistor values (R6, R7, R8) using a dynamic "test-in-circuit" technique.

To allow the digital automation of this process and ensure that the resistor settings remain stable, the design uses Intersil Digitally Controlled Potentiometers (XDCPs) as variable resistors. These devices are ideally suited to the "test-in-circuit" technique of setup, for fiber optic transmitter designs.

The X9258 from Intersil contains four XDCPs, each with 256 taps (steps) of resolution. This device is available with end-to-end resistances of 100 k $\Omega$  or 50 k $\Omega$ .

The block diagram in Figure 6 shows the main features of the XDCP. The wiper / tap position is changed using a "make-before-break" scheme in which the new tap position switch closes before the previous opens. This method avoids open-loop behaviour of the bias control circuit, in which the bias could be driven to dangerous levels.

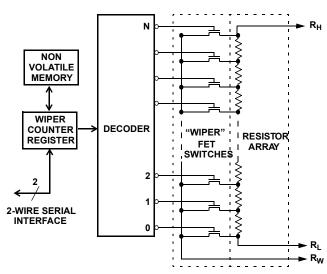


FIGURE 6. BLOCK DIAGRAM OF DIGITALLY CONTROLLED POTENTIOMETER

An industry standard 2- wire serial data bus is used to set the "wiper position" of the XDCP. Each internal potentiometer has a digital "address" to allow it to be individually commanded, and several devices may also be individually addressed on one common 2-Wire serial bus. The write protect feature of the device provides improved integrity to the settings, and also prevents tampering.

## System Design Considerations

As we can see, the Intersil XDCPs are ideally suited to the task of setting the control parameters:  $R_{PINSET}$ ,  $R_{MODSET}$ , and  $R_{BIASSET}$  of the laser diode control chipset.

Some designers may opt to use a fixed resistor (with a value slightly less than the minimum calculated in Table 4) in series with the XDCP. This removes the potentially disastrous consequence of a programming error causing a high value of current to be selected.

The resistor varies linearly with "tap position", and the steps of current for a single tap change is much greater when the tap number (and the resistance) is low (refer to Figure 7). When the tap number changes from 1 to 0, the series fixed resistor is all that limits the current. Allowance must also be made for the wiper resistance, which effectively adds to the digitally-controlled resistance value. The wiper resistance is typically 150  $\Omega$ .

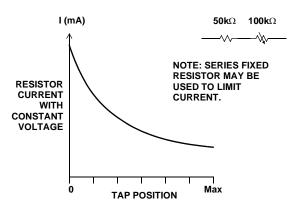


FIGURE 7. RESISTOR CURRENT AS A FUNCTION OF TAP POSITION

To achieve "the high resolution of set current", two potentiometers may be used in series. In the design example shown in the Appendix, the two ends of the potentiometer have been looped back to give a parabolic curve of resistance versus tap position. Near the center tap position, a very fine resolution may be achieved (Figure 8).

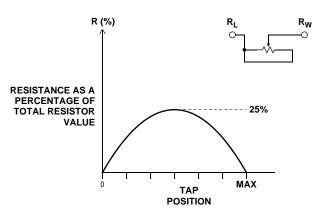


FIGURE 8. RESISTANCE vs TAP POSITION FOR BIAS CIRCUIT

The importance of maximizing resolution is that it allows the power levels to be set as closely as possible to the design values. Consider for example a system with a range of twelve equal resistor choices. In this case the bias for the '0' level can be set only in increments of 1mA, from 2.5 mA to 7.5 mA. In a worst case scenario, the '0' level could be set nearly 1 mA above the correct value, which could give a '0' level of 0.1 mW. This reduces the extinction ratio to less than 5 dB. The use of a resistor with at least 128 taps gives a resolution of 0.1 mA, giving much finer increments of optical power, and consequently greater extinction ratio.

In the above example two potentiometers are used in series. Unlike fixed resistors, only select resistance values are available for XDCPs. If the values available prove to be unworkable, the circuit in Figure 9 may be used. In this case, the XDCP is used in true potentiometer mode (voltage divider), with an analog voltage buffer and a fixed resistor. In our design example using the SY88922 however, this arrangement would reduce the effect of the temperature compensation built into the reference voltage.

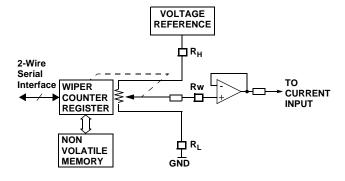


FIGURE 9. BLOCK DIAGRAM OF DCP WITH BUFFER

It should be noted that attempting to increase the optical power to near maximum (say 800  $\mu$ W) will require around 10 mA of modulation current. At this level the feedback loop has only limited range (±2mA) to control the output power.

## **Transmitter Setup Procedure**

Now that we have examined how Intersil XDCPs may be used to set the various control parameters of laser diode driver, we shall now examine the setup procedure for the completed circuit (see Appendix). The basic algorithm for setting up the circuit is as follows:

- The three resistors R6, R7 and R8 (corresponding to the parameters R<sub>BIASSET</sub>, R<sub>MODSET</sub> and R<sub>PINSET</sub>) should be set to their maximum possible values calculated above
- The feedback from the error amplifier should be opened, and an optical power meter connected to the optical fiber output

A more detailed description of the set-up procedure is described below:

## R<sub>BIASSET</sub>

With a zero on the data input lines, the value of  $R_{BIASSET}$  should be reduced from its maximum value of 17 k $\Omega$  until the desired optical power value of a '0' is achieved (around 0.035mW in this example).

#### R<sub>MODSET</sub>

The data is changed to a '1', and the value of R<sub>MODSET</sub> adjusted until the desired optical power value of a '1' is achieved (around 0.35mW in this example).

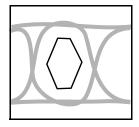
#### R<sub>PINSET</sub>

A bit pattern with the same line code as the application is applied to the data inputs, with a data rate of at least 25Mb/s [8]. The feedback control loop can now be closed [J2]. The mean optical power should fall to a much lower level as the feedback loop tries to match the optical power to the low  $I_{\text{PINSET}}$  value.

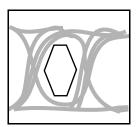
The value of  $R_{PINSET}$  is then adjusted until the optical power meter confirms the correct value is reached. With a line code yielding a 1:1 ratio ('1' vs. '0'), this will be 0.18mW. In the design example an independent op-amp 18 on "7301" also monitors the monitor photo-diode current, and gives a voltage at the test connector for future reference.

Finally, a test at the design data rate should be made to optimize the value of R<sub>BIASSET</sub> (i.e. the "0" level) for jitter and extinction ratio. The example "eye-diagrams" in Figure 10 demonstrate these points.

#### **IDEAL BIAS POINT:**



**BIAS POINT TOO LOW:** 



Jitter caused due to bias point being set too low. The final "1" in the pattern "101" rises more quickly than "1001" or "10001". The slow falling edge reduces extinction ratio.

FIGURE 10. EFFECT ON EYE DIAGRAM OF BIAS

#### Circuit Test Results

Using the circuit shown in the Appendix and following the set-up procedure detailed above, the oscilloscope trace in Figure 11 shows the actual received signal.

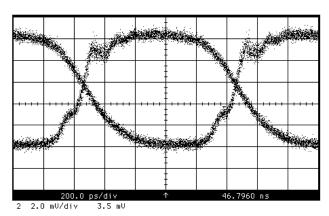


FIGURE 11. OSCILLOSCOPE TRACE OF RECEIVED SIGNAL AT 1Gb/s

The test conditions / test set-up used for obtaining this trace were as follows:

- 62.5μm optic fiber, 3m in length
- Newport D70xr optical detector, with a rise time of 70ps
- 1Gb/s data rate with a "101010" pattern

No low-pass optical filter (after the detector) was used.

## Intersil Development Tools

Intersil provides a complete programming development tool (Intersil Part Number: **XLABVIEW01**) based on the LabView<sup>™</sup> platform.

This development package combines the required software graphical user interface (GUI) and computer interface hardware, and enables the designer to quickly and easily control any of the devices in the Intersil Digitally Controlled Potentiometer (XDCP) family.

Furthermore, the development tool provides the low level LabView™ software driver required to manipulate all Intersil XDCP products. In the case that a designer utilizes LabView in their existing manufacturing environment, these low level drivers may be freely incorporated into "set-on-test" programs.

The Intersil XDCP LabView™ development tool software may be downloaded free of charge, from the Intersil Web Site at the URL address http://www.intersil.com.

#### References

- 1. Saleh and Teich, "Fundamentals of Photonics", Wiley 1991, pp 905-906.
- Honeywell Optoelectronics Application Sheet, "Modulating VCSELS", Jim Tatum and Jim Guenter, p.11
- Honeywell Optoelectronics Application Sheet, "Modulating VCSELS", Jim Tatum and Jim Guenter, figure 2
- 4. Honeywell Optoelectronics Application Sheet, "VCSEL Optical Characteristics", p1.
- Honeywell Optoelectronics Application Sheet, "Modulating VCSELS", Jim Tatum and Jim Guenter, figure 9
- Honeywell Optoelectronics Application Sheet, "High Speed characteristics of VCSELs", Jim Tatum et al, figures 8, 9 &10
- Honeywell Optoelectronics, Honeywell VCSEL Manufacturability", 8 Aug 2000, p.1
- Honeywell Optoelectronics Application Sheet, "Modulating VCSELS", Jim Tatum and Jim Guenter, figure 6.

## **Bibliography**

- · Intersil X9258 Data Sheet
- · Intersil AN137 Application Note
- · Micrel-Synergy SY88922 Data Sheet
- Micrel-Synergy SY88905 Data Sheet

## Sites of Interest

- Intersil Inc. (http://www.intersil.com)
- Micrel-Synergy (http://www.micrel.com)

Application Note 140

## **Application Note 140**

## Appendix B

TABLE 5. Parts List for Laser Diode Driver

DESIGNATOR	PART TYPE	DESCRIPTION
C1, C2, C3	1000μF/16V	Electrolytic radial 0.5" diam x 1"
C13, C14a, C15, C20, C22	1nF	High frequency decoupling type NPO
C14b	10nF	Decoupling type X7R
C18, C19	100nF	Decoupling type X7R
C4, C5, C6	4.7μF Tant	Tantalum surface mount case 'B'
C7, C8, C9, C10, C12, C16, C17, C21	0.1μF	Decoupling type X7R
J1	CON10	Power connector
J2	CON2	Feedback jumper link
J2, J3	COAX	PECL Signal connector
LD1	HFE4380-321	VCSEL Laser diode
R1, R2	82R	Resistor
R10	500R	Resistor
R11, R14	10K	Resistor
R12, R13	560K	Resistor
R16, R17, R18, R19	47K	Resistor
R20, R21, R22, R23, R5a, R5b	47R	Resistor
R28	91R	Resistor
R29, R30	390R	Resistor
R3, R4	130R	Resistor
R6, R7, R8	See text on page 6	Resistor
U1	7905	Linear regulator
U2, U3	7805	Linear regulator
U4	SY88905	Laser diode controller
U5	SY88922	Laser diode driver
U6, U7	X9258TS24I-2.7	Intersil DCP array
U8	7301	Opamp

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.